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# A Novel Low Power Gate Driver Architecture for Large 8K 120Hz LCD Display Employing IGZO Technology

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## Abstract

***A novel low power gate driver architecture was developed for large 8K 120Hz LCD panel. For this application, not only high speed driving but also low power consumption is required. We employed a high mobility IGZO, dual $V_{GL}$ level driving method and gate driver circuit driven by DC supply. The simulation results show that our proposals meet 8K 120Hz driving requirements. Also, we have fabricated a prototype panel and confirmed high speed driving and low power consumption.***

## Author Keywords

IGZO; Oxide TFT; GIP; 8K; Low Power Consumption

## 1. Introduction

Not only small and middle size displays but also large sizes such as 80-inch class displays require Gate Driver in Panel (GIP) architecture for design and cost reduction purposes. Because of the high resolution and heavier load, GIP design should be considered in the interest of high-speed driving and low power consumption.

In order to achieve high-speed driving for an 8K 120Hz display, not only reducing the gate bus line load but also a new driving method is required for faster gate fall time. Although we have developed a 1st and 2nd Gen. IGZO (Etch Stopper (ES) type) and a 3rd and 4th Gen. IGZO (Channel Etch (CE) type) [1][2], we have newly developed a 5th Gen. IGZO of higher mobility. It brings us the benefits of a load reduction for high-speed driving. And, we also employed dual $V_{GL}$ level driving to speed up gate fall time.

Various types of GIP circuits that charge the gate bus line with clock signal ("conventional type") have been developed [3][4]. But, they are unsuited for low power consumption because of the increase in TFT size due to panel enlargement. On the other hand, a circuit that drives the gate bus line with DC supply ("DC buffer type") has been proposed [5]. This type is suitable for low power consumption, especially for large scale panels with heavy load.

We confirmed that a large 8K 120Hz display can be realized with the newly developed IGZO TFT and new circuit architecture.

## 2. Electrical Characteristics of IGZO TFT

Figure 1 shows the Id-Vg characteristic of the 5th Gen. IGZO TFT. Structurally, the TFT is of channel etch type with a bottom gate. The mobility is 15 $cm^2/V{\cdot}s$ or more.

TFT sizes of the GIP circuit must be designed in consideration of the $V_{TH}$ shift caused by gate stress. Figure 2 shows the measurement results of the $V_{TH}$ shift by positive BT for a-Si, the 2nd Gen. IGZO and the 5th Gen. IGZO. As the generation progresses, the $V_{TH}$ shift value becomes smaller. The $V_{TH}$ shift value of the 5th Gen. IGZO is no more than 20% that of a-Si and 40% that of the 2nd Gen. IGZO. This means that the 5th Gen. IGZO keeps $I_{ON}$ higher even after aging. Moreover, the originally equipped higher mobility makes TFT sizes smaller and minimizes the gate load and parasitic capacitance of TFTs.

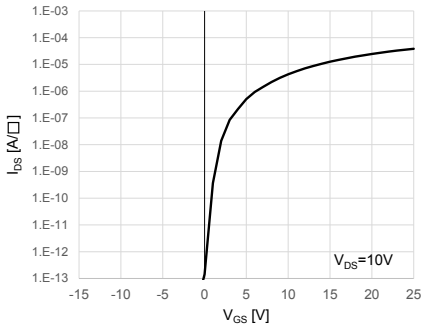


**Figure 1.** Characteristic of the 5th Gen. IGZO TFT

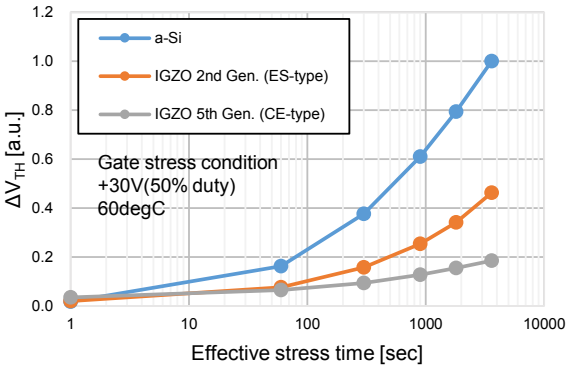


**Figure 2.** $\Delta V_{TH}$ in positive bias condition

## 3. Circuit Design

### 3.1. Proposed Circuit and Operation

Figure 3 shows the unit circuits of GIP. Figure 3(a) is the conventional type and (b) is the proposed DC buffer type.

The conventional type circuit consists of 8 TFTs (T1~T8) and one capacitor (C1), and has one output node (Gout). The DC buffer type circuit consists of 11 TFTs (T1~T8, T3A, T7A, T8A) and one capacitor (C1), and has two output nodes (Gout, Qout) and VSS has two $V_{GL}$ levels. Figure 4 shows the block diagram for DC buffer type circuit. As shown in Figure 4, Gout is connected to the gate bus line and Qout is connected to the set / reset terminal.

The circuit operation is described as followings according to the timing chart by SPICE simulation shown in Figure 5.

(a) Non-selected period

Node netB is pulled up to 'H' level by T5. The noises to node netA, Qout and Gout caused by GCK are canceled by T4, T7 and T7A, respectively. In this period, the voltages of node netA and Qout are $V_{GL2}$, and the voltage of Gout is $V_{GL}$. Note that $V_{GL} > V_{GL2}$

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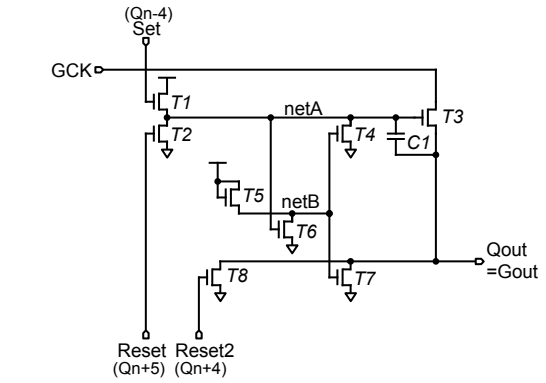
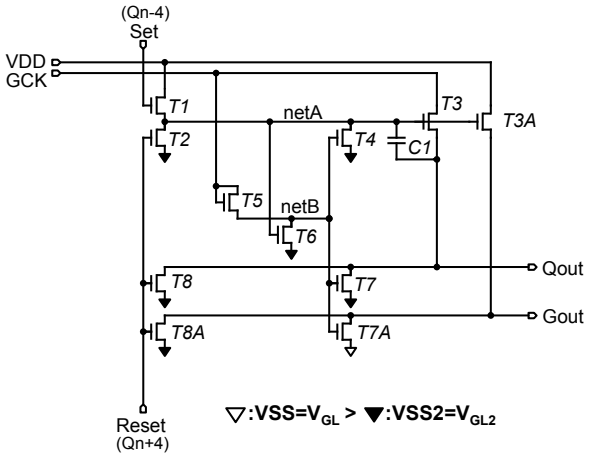



(a) Conventional type circuit




(b) DC buffer type circuit

**Figure 3.** Schematic of unit stage

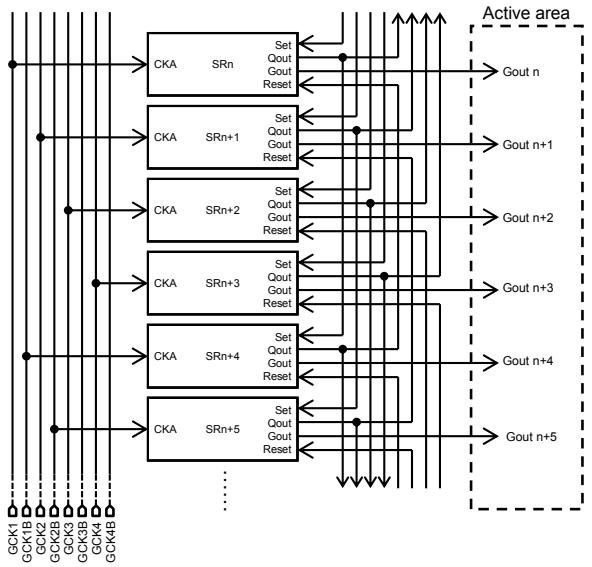



**Figure 4.** Block diagram of the shift register

(b) Set period
The Set signal (=Qout<n-4>) turns T1 on. Then, node netA is pre-charged. At the same time, T4 is turned off by T6 turning on and pulling netB down. As the voltage of node netA rises, Gout also rises.

(c) Output period
In this period, GCK rises from $V_{GL2}$ to $V_{GH}$. Node netA is boosted by C1 and the parasitic capacitance of T3. Since the voltage of node netA becomes higher than $V_{TH}$ of T3A, the voltage of Gout becomes completely $V_{GH}$. And, Qout is output at the same time.

(d) Reset period
The Reset signal (=Qout<n+4>) turns on T2, T8 and T8A. These TFTs pull node netA, Qout and Gout down to $V_{GL2}$, respectively

(e) Gout recovery period
After the reset period, GCK rises to $V_{GH}$ and turns T5 on. Node netB is pulled up to 'H' level again, and turns T4, T7 and T7A on. The voltage of Gout is recovered from $V_{GL2}$ to $V_{GL}$ by T7A.

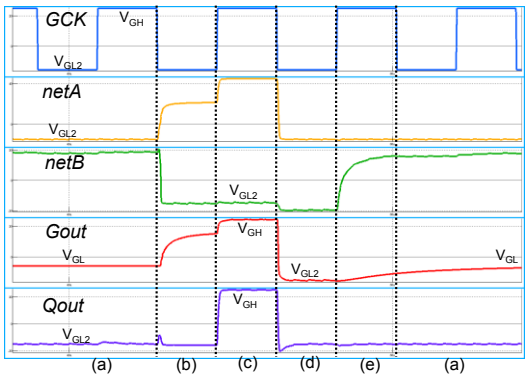



**Figure 5.** Timing chart of the DC buffer type

## 3.2. Circuit Design

Table 1 shows the panel specifications to be studied.

**Table 1.** Specification of the estimated panel

| | |
|---|---|
| Panel size | 80-inch |
| Resolution | 8K (7680RGB x 4320) |
| Frame rate | 120Hz |
| GIP Configuration | both side input |
| Source configuration | single side input<br>single source line |
| GCK phase & duty | 8phase, 50% duty |
| Pixel structure | VA |
| GIP Voltage | 25V / -6V / -16V (T.B.D.) |

### *High-Speed Driving*

In the case of the conventional circuit, Gout is discharged through T3 and T8 to 'L' level. On the other hand, the DC buffer circuit only discharges Gout to 'L' level through T8A. So, T8A is essential to the circuit and the gate fall time depends just on the channel width of T8A. Figure 6 shows the relationship between the channel width of T8A and the gate fall time by SPICE simulation. Note that $V_{GL}$=$V_{GL2}$ in this simulation. As the channel width of T8A increases, Gout falls faster. But it is not enough for the target.

In this paper, the gate fall time is defined as the time from GCK starting to fall to pixel TFT off voltage is reached.

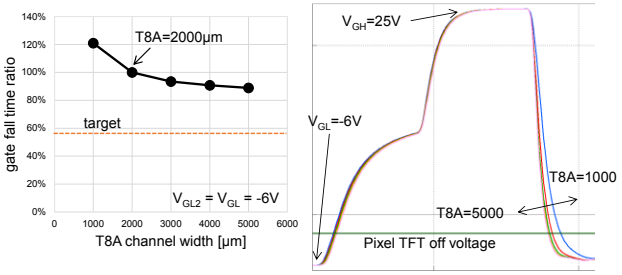



**Figure 6.** Gate fall time vs. T8A channel width and Gout waveform

Here, to speed up the gate fall time, dual low voltage is used. Figure 7 shows the relationship between the gate fall time and the $V_{GL2}$ voltage by SPICE simulation. By lowering the $V_{GL2}$ level, the gate fall time drastically decreased. From this simulation result, when the $V_{GL2}$ voltage is set lower than $V_{GL}$ by 7V, it looks good for satisfying the target.

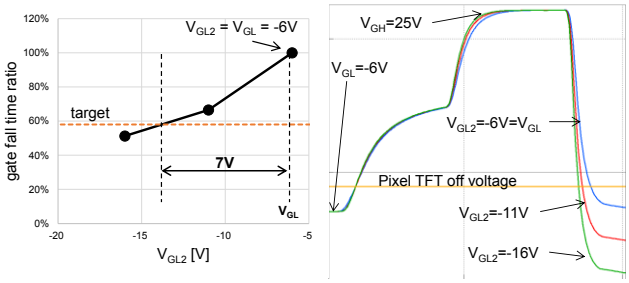



**Figure 7.** Gate fall time vs. $V_{GL2}$ voltage and Gout waveform

### *Low Power Consumption*

Next, we consider the power consumption. In the case of the conventional type, the dynamic power (Pd(conv)) is

$$Pd(conv) \propto 2\times(m\times((n\times C_{T3})+C_{CR})\times V_{GPP}^2\times f)) + P_{CG} \quad (1)$$

where the power for charging and discharging the gate bus line is $P_{CG}$, the parasitic capacitance of T3 is $C_{T3}$, the frequency of GCK is f, the number of GCK phases is m, the (parasitic) cross-capacitance between GCK and other signal lines is $C_{CR}$, the number of stages per GCK is n, and the voltage amplitude of GCK is $V_{GPP}$.

Also in the case of the DC buffer type, the dynamic power (Pd(dcbuf)) is calculated as follows;

$$Pd(dcbuf) \propto 2\times(m\times((n\times C_{T3})+C_{CR})\times V_{GPP}^2\times f)) + 2\times((m\times n\times C_{T3A}\times V_{GPP}^2\times 0)) + P_{CG} \quad (2)$$

where the parasitic capacitance of T3A is $C_{T3A}$.

In the case of the DC buffer type, the source node of T3A is connected to a DC power source (f=0). So, the power consumption at T3A, which is the 2nd term in Eq.2, is zero. The power consumption at T3 is not so large because T3 drives T2, T8 and T8A in the upper stage and T1 in the lower stage. T3 in the DC buffer type circuit does not drive large loads like T3 in the conventional type circuit. Therefore, the width of T3 is much smaller than that of the conventional type. It means $C_{T3}$ in Pd(dcbuf) is much smaller than that in Pd(conv).

Based on these viewpoint, we designed the conventional and DC buffer type circuits, and compared the power consumption. Table 2 shows channel width of major TFTs and GIP voltage. The conventional type with the 4th Gen. IGZO TFT could not operate at the same voltage setting as the DC buffer type with the 5th Gen. IGZO. In order to satisfy the gate fall time, even lower $V_{GL}$ voltage is required in the conventional type.

**Table 2.** Channel width of major TFTs and GIP voltage

| | | Conventional | | DC buffer |
|---|---|---|---|---|
| IGZO | | 4th Gen. (μ=10) | | 5th Gen. (μ=15) |
| channel width | T3 | 2000μm | N/A | 300μm (GCK) |
| | T3A | ---- | | 2500μm (VDD) |
| | T8 | 2500μm | | 3000μm |
| GIP voltage | | 25 / -16V | 25 / -13V | 25 / -6 / -13V |

Figure 8 shows the results of the estimated power consumption based on the above TFT size and voltage.

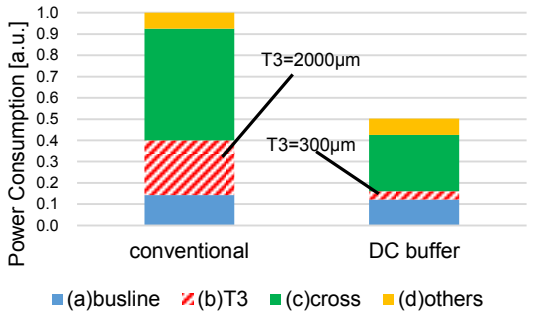



**Figure 8.** Comparison of estimated power consumption between the conventional and the DC buffer type circuits

The power consumption for driving the gate bus line (a) is of course the same. However, the power consumption in T3 driving (b) is reduced to about 1/7 as seen by the size and voltage ratios of T3. This is because, as explained earlier, T3 is smaller. In addition, since T3 is smaller, GCK wiring can be narrower. As a result, the cross-capacitance between the signal wirings also decreases and the charging and discharging power due to cross-capacitance (c) decreases. From this estimation, we have found that the DC buffer type can reduce the power consumption of large 8K displays by 50% compared with the conventional type.

Figure 9 shows the layout of the DC buffer type circuit for 80-inch display. The border width is estimated at 5.0 mm approximately.

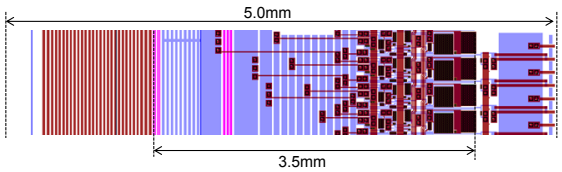



**Figure 9.** GIP layout for large display

## 4. Evaluation by Prototype Panel

In order to verify the circuit operation of the DC buffer type circuit, a small prototype panel was fabricated and evaluated. Figure 10 shows a photograph of the GIP circuit.

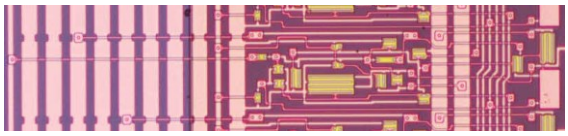
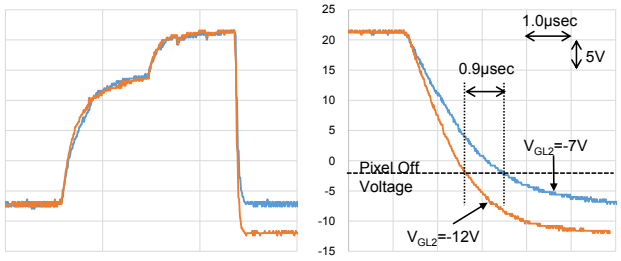


**Figure 10.** GIP circuit on the prototype panel

### 4.1. Gate Fall Time

Figure 11 shows the waveforms of Gout observed with an oscilloscope. As expected, a lower $V_{GL2}$ makes gate falling faster.




(a) Gout waveform (b) Enlarged view

**Figure 11.** Observed Gout waveforms of the prototype panel

### 4.2. Power Consumption

Table 3 shows the channel width of major TFTs, operating voltage and measured GIP power consumption of the prototype panel

**Table 3.** Comparison table of major TFT sizes, GIP voltage and GIP power consumption on test panel

| Circuit | | Conv. #1 | Conv. #2 | DC buffer |
|---|---|---|---|---|
| Device size | T3 | 260μm | 400μm | 25μm |
| | T3A | ---- | ---- | 100μm |
| | T8 | ---- | ---- | 240μm |
| GIP voltage | | 21/-12V | | 21/-7/-12V |
| Total GIP Power | | 33.3mW | 36.9mW | 27.7mW |

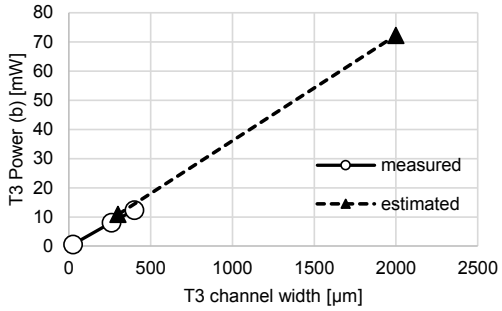



**Figure 12.** Power consumption in T3

Figure 12 shows the result of comparing the measured power consumption of the prototype panel in T3 driving and the estimated power (b) from Figure 8. The estimated power consumption was converted for comparison. Both the measured and estimated power consumption (b) were plotted on the same line, so the accuracy of the power consumption estimate for the DC buffer type circuit was confirmed to be correct.

From the above, we confirmed that the DC buffer type circuit with the 5th Gen. IGZO TFT operates as assumed for both high speed and low power consumption.

## 5. Conclusion

We have developed a novel circuit architecture with IGZO TFT to solve conflicting issues of high-speed driving and low power consumption for large 8K 120Hz display. They can be realized with the (1) performance-enhanced 5th Gen. IGZO TFT, (2) dual $V_{GL}$ level driving method and (3) DC buffer type circuit. In order to verify the circuit operation, a prototype panel was fabricated and we have confirmed it operates with low power consumption as expected. Figure 13 shows a photograph of a prototype panel.

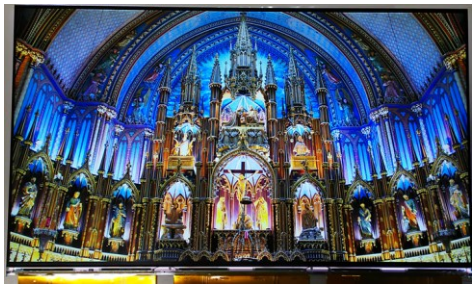


**Figure 13.** Prototype panel with proposed gate driver

## 6. Acknowledgements

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